

A New Multilevel Inverter Topology to Drive an Induction Motor System

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ABSTRACT: For the driving of an induction motor, we need high quality AC power. Therefore, an inverter is required to convert the DC power supply to AC. To increase the quality of the AC power we have to increase the number of levels of the inverter. However, with the conventional multilevel inverters, the number of switches and other associated components are also increases in a huge amount, with the increase of each level. Thus, the overall loss of the inverter is also increases, which hampered the smooth running of the induction motor tremendously. Therefore, for smooth running of an induction motor, it should be driven by a multilevel inverter, which can produced large number of AC power levels with less number of switches. In this paper, a new approach of designing multilevel inverter is proposed, which can generate Nine-levels of output voltage with only eleven switches. This paper also shows the smooth running of a single-phase induction motor by the newly designed reduced number of switch multilevel inverter.

KEYWORDS: Multilevel Inverter, Level generator section, Polarity changer section, H-Bridge, IGBTs with anti-parallel diode, MATLAB SIMULINK, SPWM.

I. INTRODUCTION

For pumps, smaller fans, blowers, short belt conveyors, machine tools such as drills, lathes single-phase induction motors are well suited for their limited size. However, the fact is that, we must need an inverter to convert the DC power supply to AC, to drive the induction motor. If the quality of the output power of the inverter is low it causes high THD and creates disturbances in the running of the induction motor. That's why, for high quality AC power supply for the induction motor, we need a multilevel inverter with large numbers of output levels. There are three conventional multilevel inverter topologies (i) Diode Clamped (DC) (ii) Flying Capacitor (FC) and (iii) Cascaded H-Bridge (CHB) [1],[2],[3]. These three conventional multilevel inverter topologies are shown in figure 1.

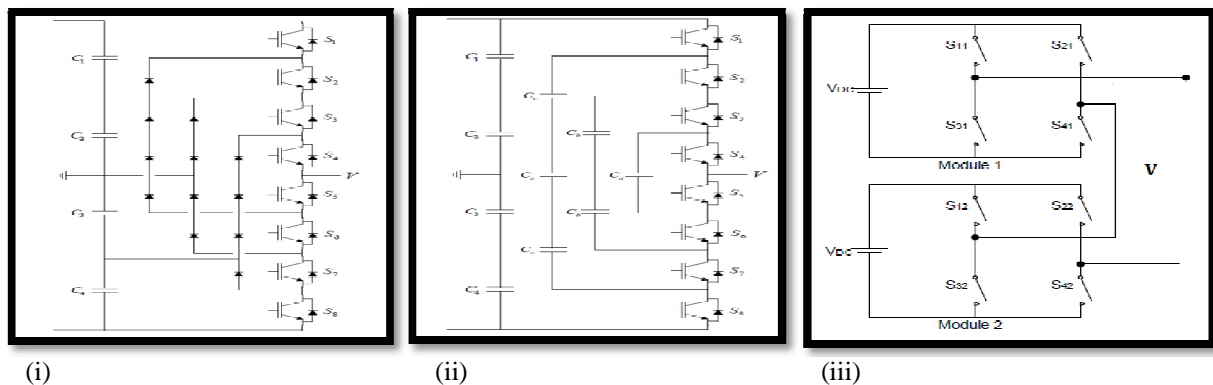


Fig. 1. 5 Level (i) Diode Clamped (DC) Inverter (ii) Flying Capacitor (FC) Inverter and (iii) Cascaded H-Bridge (CHB) Inverter

International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 5, Issue 4, April 2016

But the problem with these conventional multilevel inverters is that, as the number of level increases it requires more number of power switches, clamping diode, flying capacitor and associated components respectively. Thus the losses, installation area and cost of the inverter and simultaneously the installation area and cost of the induction motor increases to a huge extent. Therefore, for smooth running of an induction motor efficiently with low cost and reduced installation area, we have to overcome the problem of using large number of switches in conventional multilevel inverters. With the designing of a new multilevel inverter with reduced number of switches, this paper takes a step forward to the development of multilevel inverters family to a large extent without hampering the output voltage quality. For the last few years many researchers take initiative in the field of reduced switch multilevel inverter [4],[5] but this paper demonstrate the best possible design of the higher level multilevel inverter topology with less number of switches in the field of induction motors.

II. PROPOSED TOPOLOGY

The proposed topology consists of two portions; one portion called level generator and another one is called polarity changer. The Proposed topology designing multilevel inverter is shown in figure below. The level generator and polarity changer part is marked in the figure.

A. Proposed Circuit Analysis

In level generator section when gate signal is given only to switch S1, then voltage V_{dc1} is appeared across the load of the polarity changer portion of the inverter circuit. In this case, conduction of current is take place through switch S1 and anti-parallel diodes of the switches S5, S6 and S7. Similarly, when gate signal is given only to switch S2, conduction of current take place through the switch S2, and anti-parallel diodes of the switch S5 and S6 and voltage $(V_{dc1}+V_{dc2})$ appears across the load of the polarity changer circuit; when gate signal is given only to switch S3, conduction of current take place through the switch S3 and anti-parallel diodes of the switch S5 and voltage $(V_{dc1}+V_{dc2}+V_{dc3})$ appears across the load of the polarity changer circuit; when gate signal is given only to switch S4, conduction of current take place through the switch S4 and voltage $(V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4})$ is appeared across the load of the polarity changer portion of the inverter circuit.

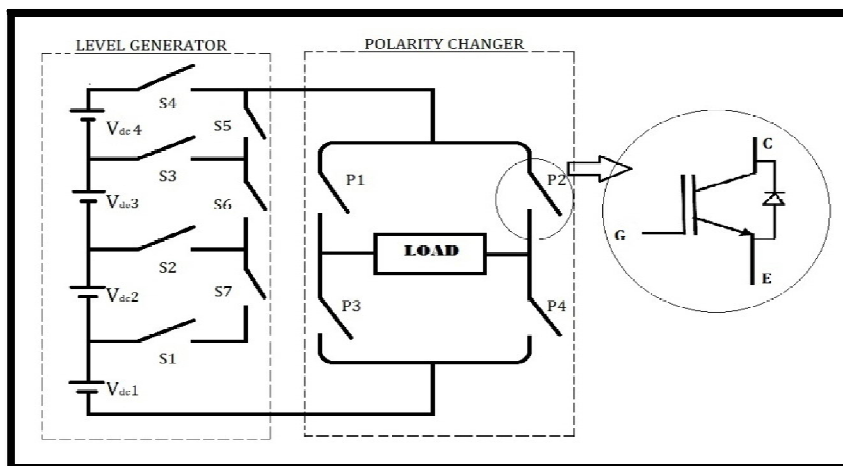


Fig. 2. Proposed 9-Level Inverter with R-L Load Using Only 11-Switches

In the polarity changer portion the circuit is composed of four power switches (i.e., IGBTs). This circuit is also called H-bridge circuit. The only condition is that, the same switches in same leg should not be turned on simultaneous in order to avoid the short circuit with DC source. The operational logic behind the polarity changer portion is that, when (P1, P4) are on and (P2, P3) are off, the load voltage is positive; whereas, in the case of (P1, P4) are off and (P2, P3) are on, the load voltage is negative.

International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 5, Issue 4, April 2016

Both the positive and negative levels synthesized by the H-bridge circuit, at resistive load (V_o , Load) synthesized stepped output voltage level will be obtained as

$$V_o = \begin{cases} \sum_{i=1}^m V_{dci} & , P1, P4 = 1 \\ \sum_{i=1}^m -V_{dci} & , P2, P3 = 1 \end{cases}$$

Here, gate signal is given to the switches S5, S6 and S7 at the time when S1,S2,S3,S4 are off i.e. when voltage level across the load of the inverter is zero, at that time these switches gives free-wheeling path to the stored energy in the load due to inductance.

9-level proposed multilevel inverter

In a 9-level proposed multilevel topology:

$n=9$

Therefore:

Number of DC voltage sources = $(n-1)/2 = 4$

Number of switches = $n + 2 = 11$

B. Switching States of Proposed Topology

The on-state and off-state of the switches, for different voltage levels across the load is shown in a table form below.

TABLE I
SWITCHING STATES OF 9-LEVEL PROPOSED

Switching States											Voltage Level at $V_{O, Load}$
S1	S2	S3	S4	S5	S6	S7	P1	P2	P3	P4	
1	0	0	0	0	0	0	1	0	0	1	V_{dc1}
0	1	0	0	0	0	0	1	0	0	1	$V_{dc1}+V_{dc2}$
0	0	1	0	0	0	0	1	0	0	1	$V_{dc1}+V_{dc2}+V_{dc3}$
0	0	0	1	0	0	0	1	0	0	1	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$
0	0	0	0	1	1	1	1	1	0	0	0
1	0	0	0	0	0	0	0	1	1	0	$-V_{dc1}$
0	1	0	0	0	0	0	0	1	1	0	$-(V_{dc1}+V_{dc2})$
0	0	1	0	0	0	0	0	1	1	0	$-(V_{dc1}+V_{dc2}+V_{dc3})$
0	0	0	1	0	0	0	0	1	1	0	$-(V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4})$

III. MATLAB SIMULATION

A. MATLAB Simulation Model of Proposed Inverter Topology

Proposed inverter model for 9-level with only 11 switches is designed using MATLAB SIMULINK and is shown in the figure 3. For designing this circuit we used 11 IGBTs as switches and 4 dc voltage sources each rated with 100 V. As we all know that, for turning on IGBT we have to give a pulse signal on IGBT gate terminal. Here for gate pulse of eight IGBTs (P1, P2, P3, P4, S1, S2, S3 and S4) we used Sine Pulse Width Modulation technique and for the gate pulse of the three switches S5, S6 and S7, we used pulse generators. We design the proposed model for R-L load where, $R=10$ ohm & $L=60$ mH is connected in series across the load in the simulation model.

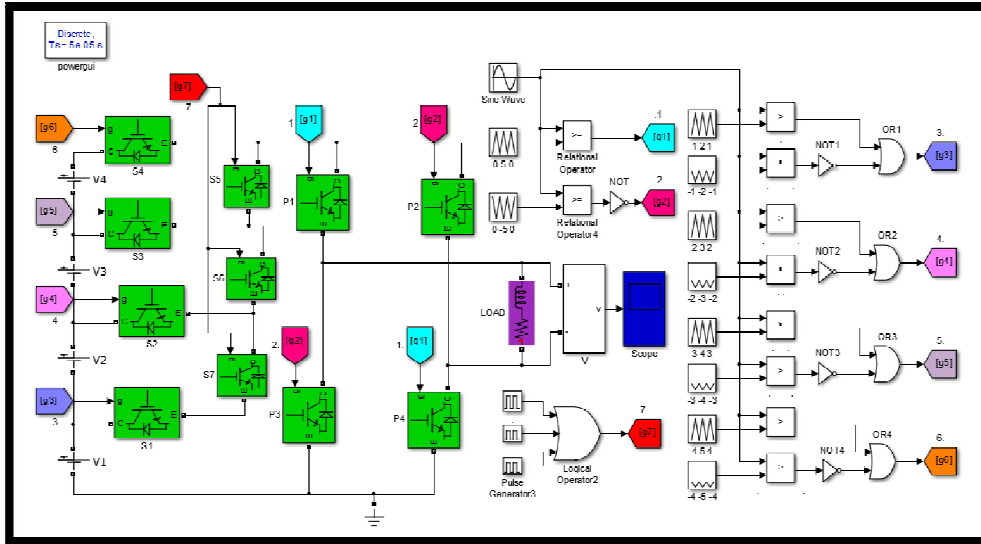


Fig. 3. MATLAB Simulation Design of 1-Phase 9-Level Inverter for R-L Load

B. Implementation of the proposed inverter

The proposed inverter model is used to drive a single-phase capacitor start capacitor run induction motor, shown in the figure 4. The parameters of the capacitor start capacitor run induction motor used in this simulation model is listed below.

Main winding of the stator has 2.02 ohm resistance and 7.4 mH inductance.

Main winding of the rotor has 4.12 ohm resistance and 5.6 mH inductance.

Main winding mutual inductance: 0.177 H.

Auxiliary winding of the stator has 7.14 ohm resistance and 8.54 mH inductance.

Capacitor-Start has 2.15 ohm resistance and 255 μ F capacitance.

Capacitor-Run has 18 ohm resistance and 21.1 μ F capacitance.

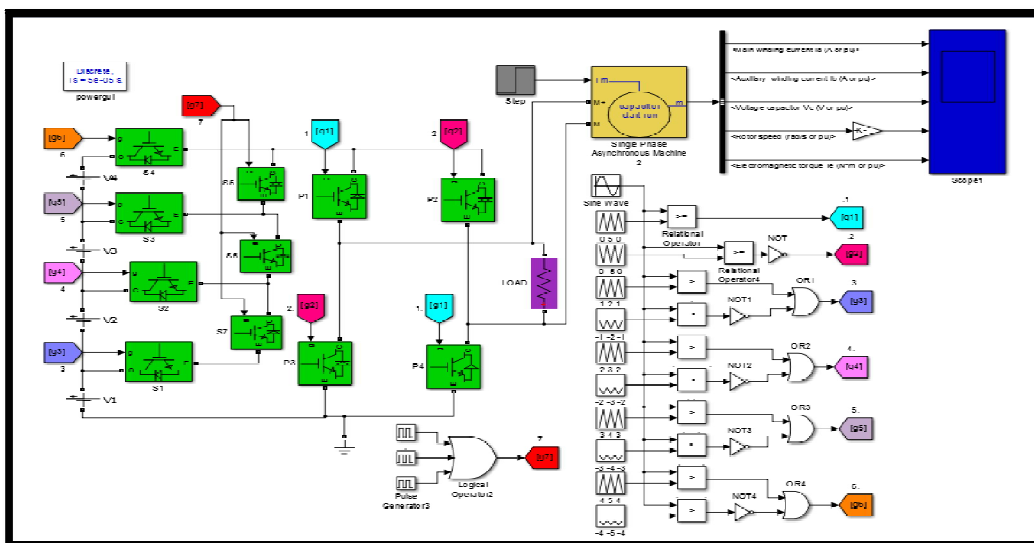


Fig. 4. Proposed Inverter Topology with a Capacitor Start Capacitor Run Induction Motor as a Load

IV. SIMULATION RESULTS

A. MATLAB Simulation Result of Proposed Inverter Model

After running the MATLAB simulation model shown in figure 3, the visible single-phase 9-level approximately sinusoidal output voltage graph with respect to time is appear in the scope, which is shown in the figure 5.

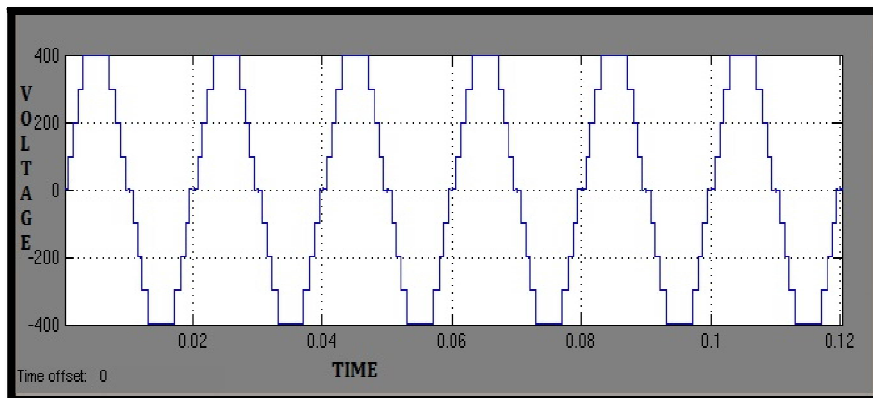


Fig. 5. 1-Phase 9-Level Output Voltage Simulation Result for R-L Load

B. MATLAB Simulation Result of the Induction Motor

After running the MATLAB simulation model shown in figure 4, the visible graph of main winding current I_a , auxiliary winding current I_b , voltage capacitor V_c , rotor speed, electromagnetic torque T_e of the single-phase capacitor start capacitor run induction motor with respect to time is appear in the scope, which is shown in the figure 6.

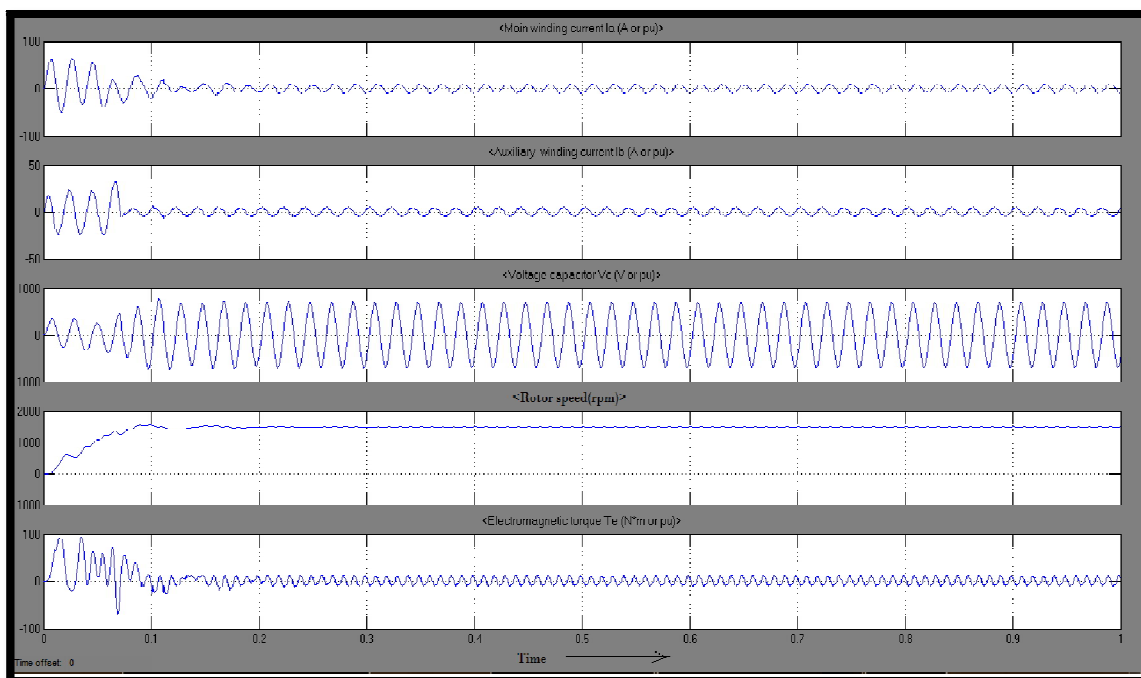


Fig. 6. Main Winding Current, Auxiliary Winding Current, Voltage Capacitor, Rotor speed and Electromagnetic Torque of the 1-Phase capacitor start capacitor run Induction Motor

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V. CONCLUSION

In this paper, a new approach of designing multilevel inverter is proposed, which uses reduced number of switches. As the number of power switches are reduced here, the efficiency of the inverter is increased. The operation of the proposed 9 level inverter fed induction motor drive system is implemented and observed.

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BIOGRAPHY



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